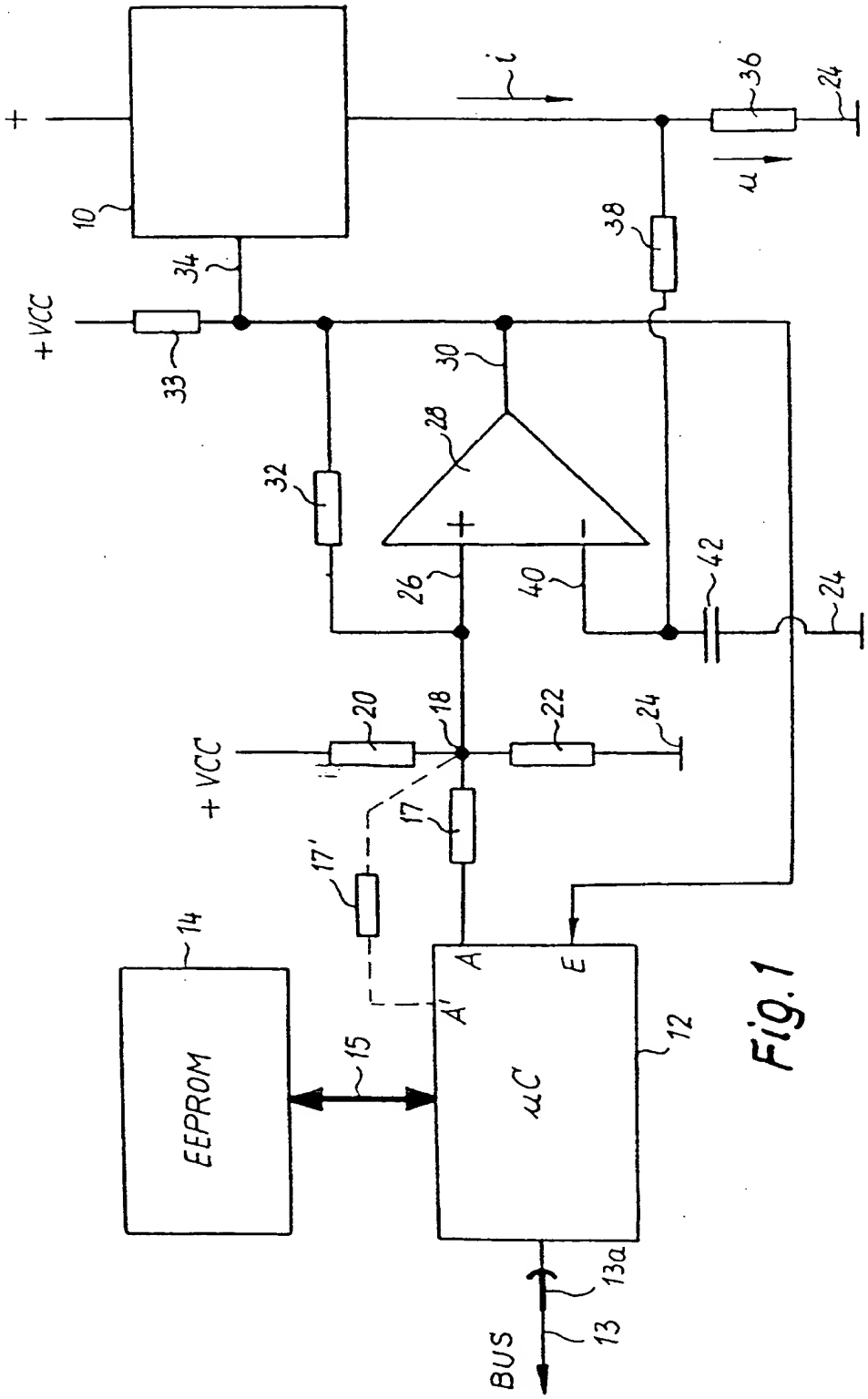
+
10
i
36
24
u
38
34
+VCC
33
30
28
32
+
-
26
40
42
24
20
18
22
24
+VCC
17
17'
14
A
A'
E
EEPROM
15
µC
12
13a
13
BUS

Fig. 1

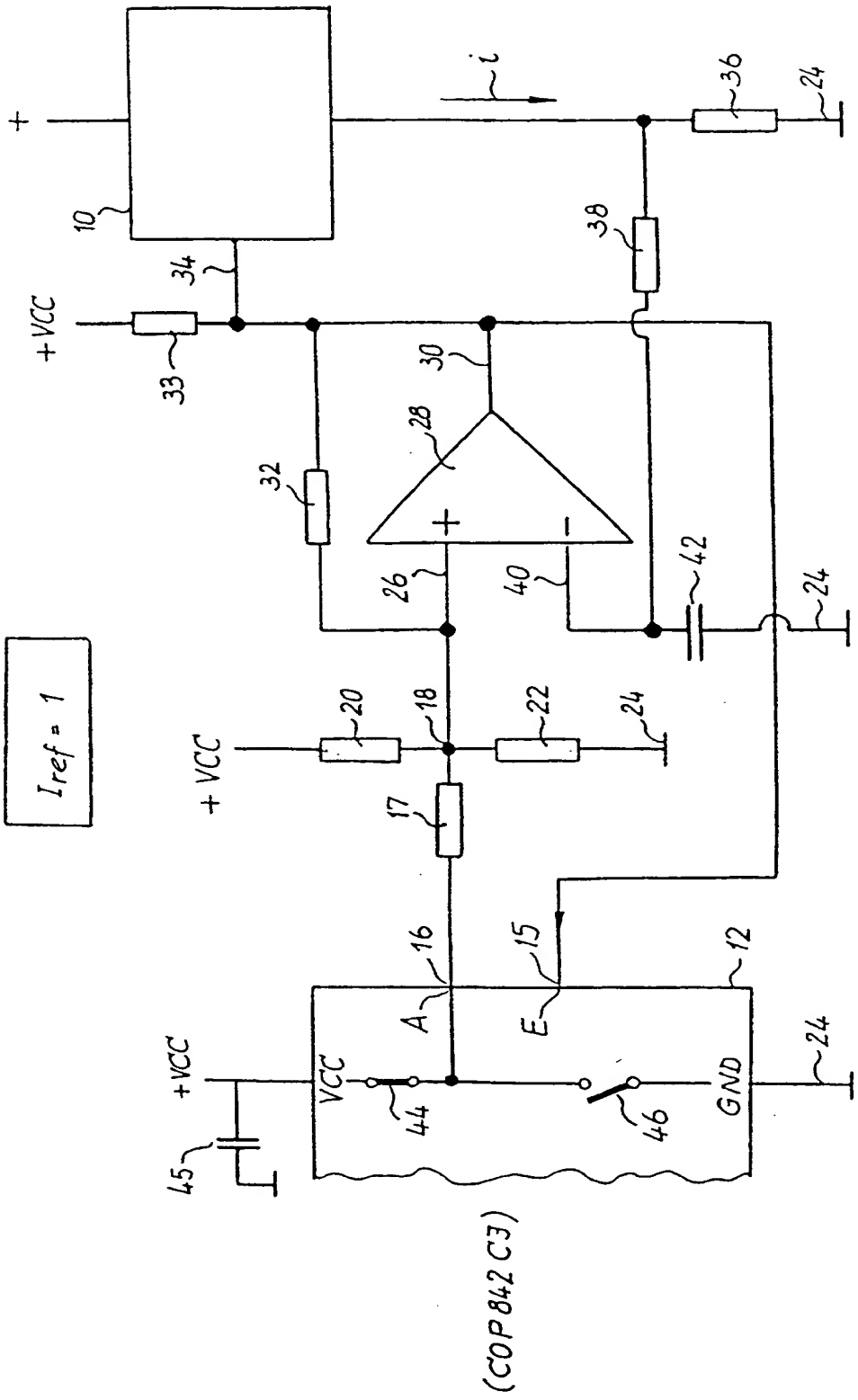
+
i
36
24
10
38
34
+VCC
33
30
28
32
26
40
42
24
Iref = 1
20
18
22
24
+VCC
17
16
15
12
A
E
+VCC
VCC
44
46
GND
24
45
(COP842 C3)

Fig. 2

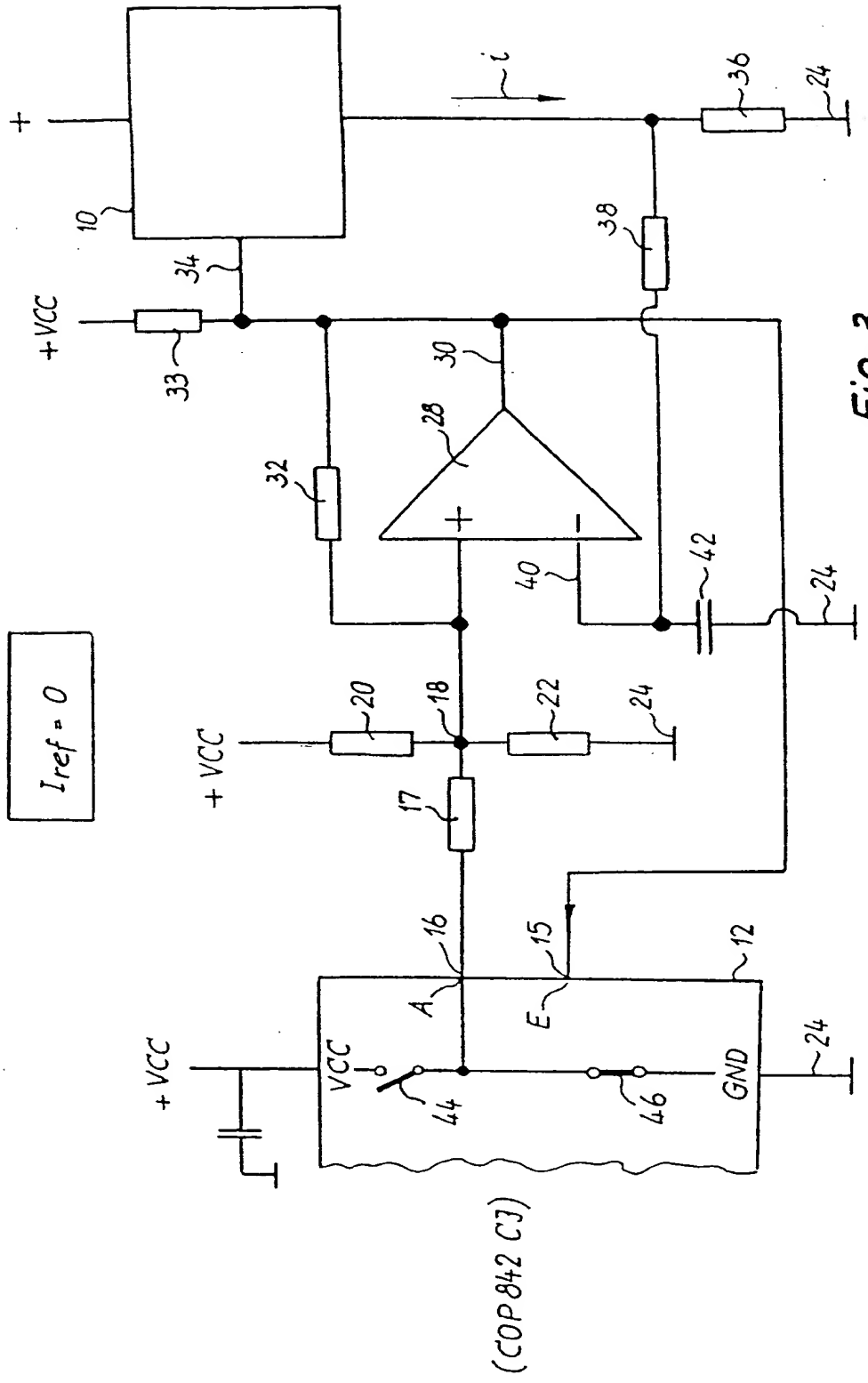

Fig.3

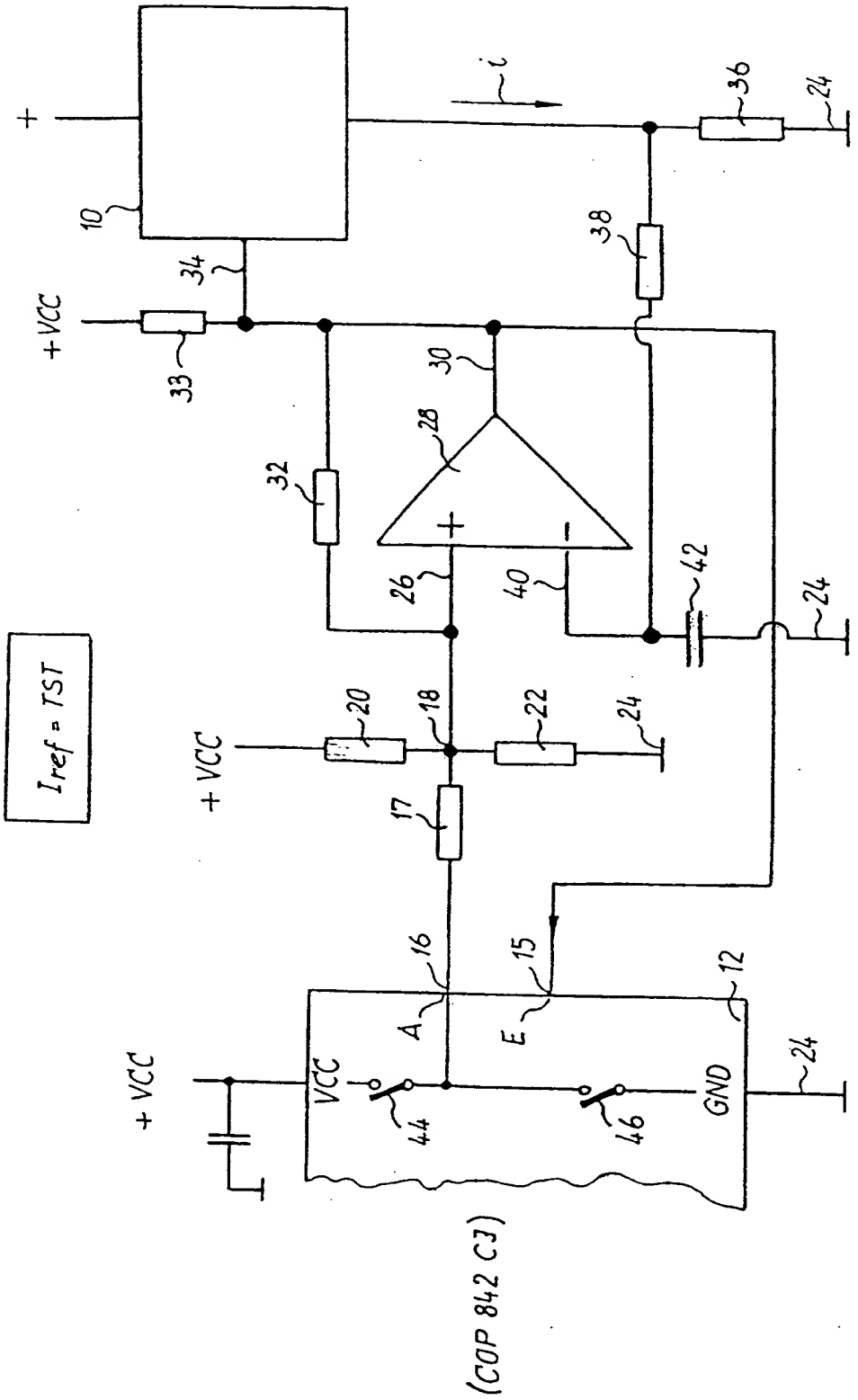
+
10
i
36
24
38
34
+VCC
33
30
28
32
26
40
42
24
Iref = TST
+VCC
20
18
22
24
17
16
15
12
A
E
+VCC
VCC
44
46
GND
24
(COP 842 CJ)

Fig. 4

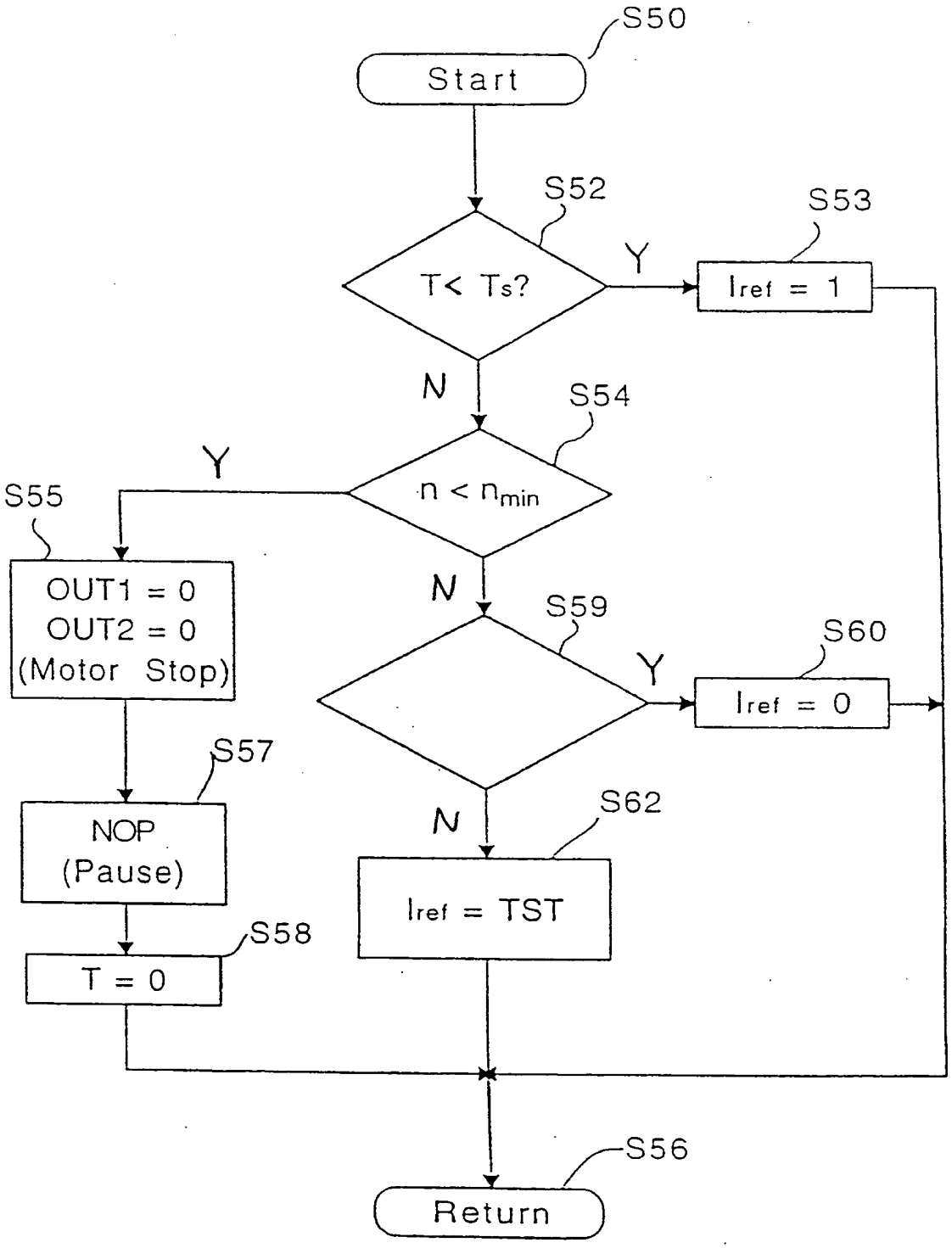
S50
Start
S52
T< Ts?
Y
S53
Iref = 1
N
S54
n < nmin
Y
S55
OUT1 = 0
OUT2 = 0
(Motor Stop)
N
S59
Y
S60
Iref = 0
S57
NOP
(Pause)
N
S62
Iref = TST
S58
T = 0
S56
Return

Fig. 5

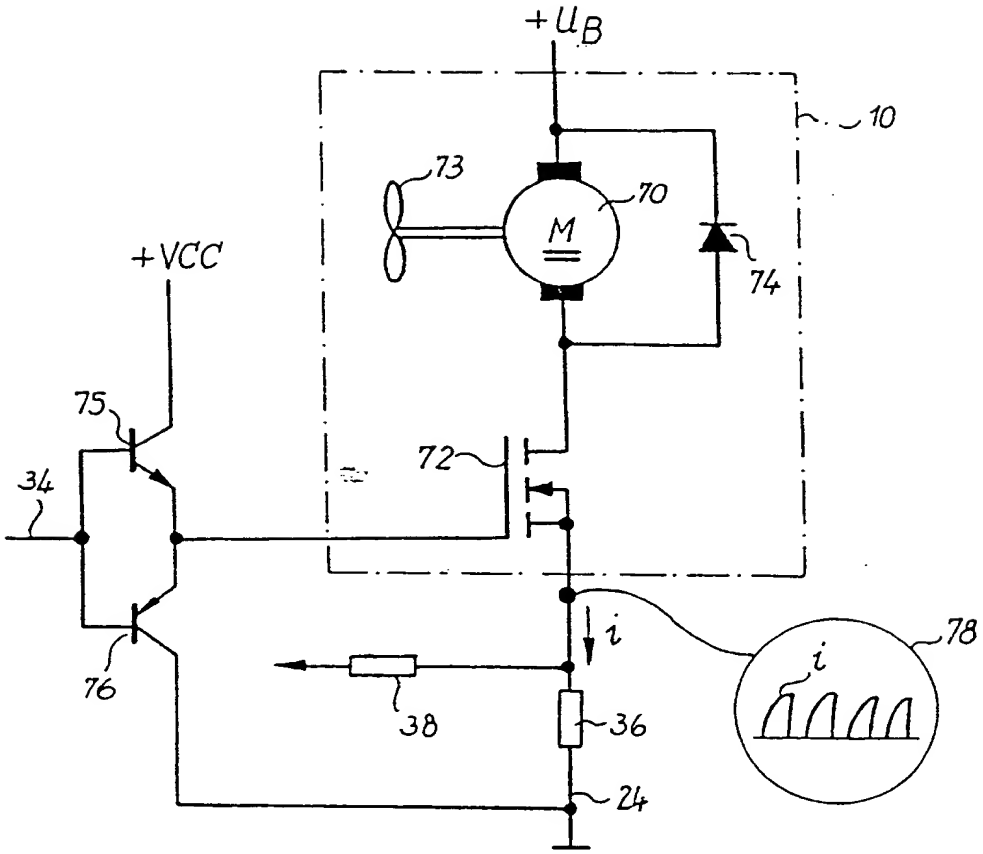

Fig. 6

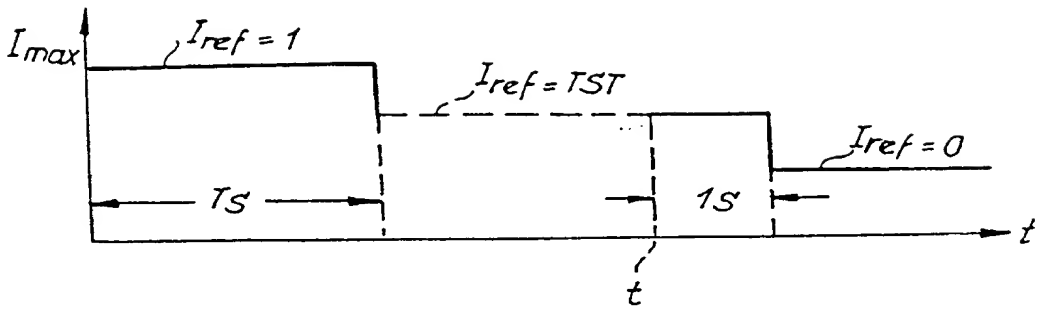
Imax
Iref = 1
Iref = TST
Iref = 0
TS
1S
t
t

Fig. 7

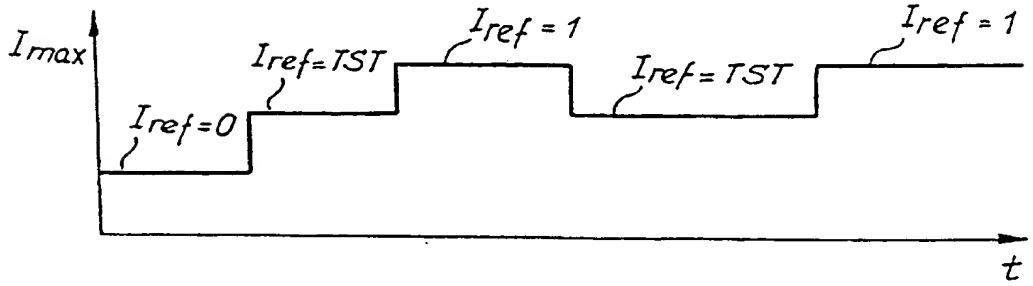
Imax
Iref = 0
Iref = TST
Iref = 1
Iref = TST
Iref = 1
t

Fig. 8

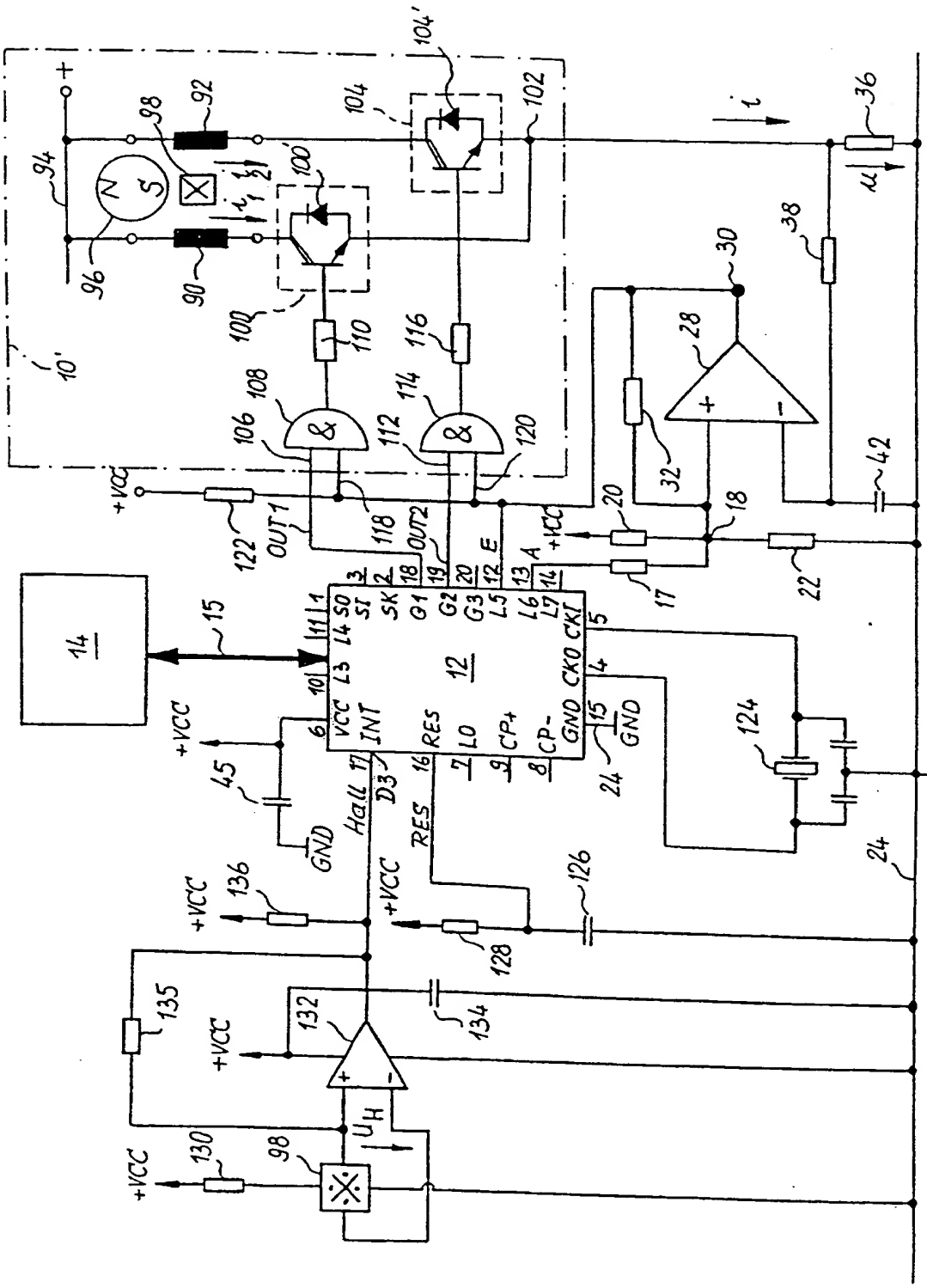
10'
14
15
12
+VCC
GND
OUT1
OUT2
Hall
RES
INT
VCC
GND
SCK
SI
SO
CKI
CKO
G1
G2
G3
L5
L6
L7
CP+
CP-
LO
A
E
U_H
i

Fig. 9

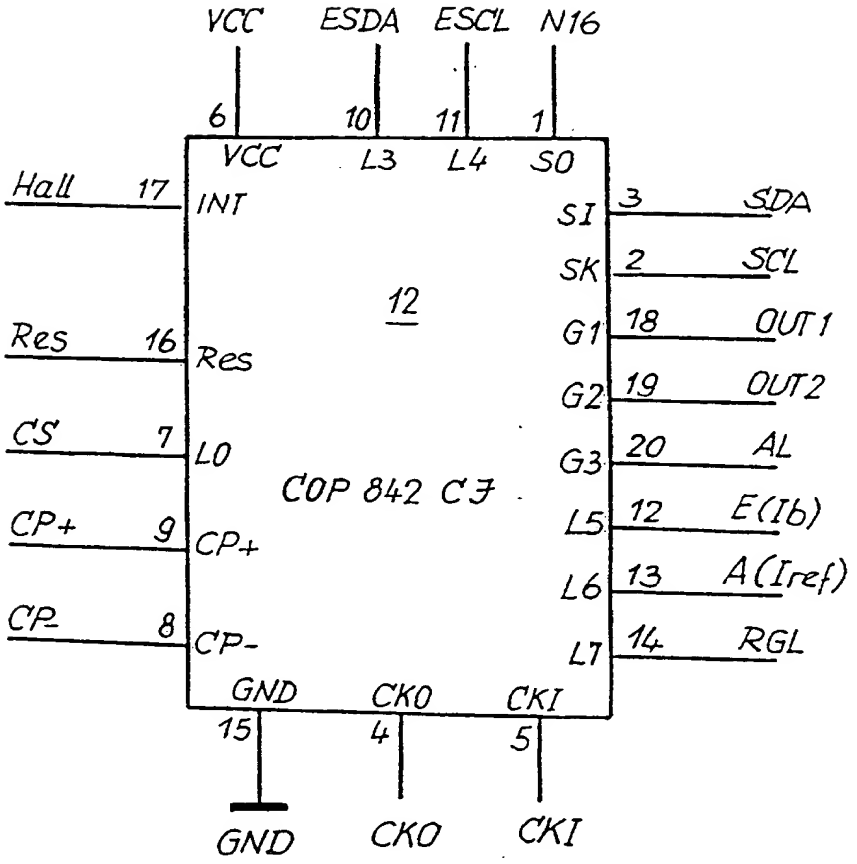
VCC
ESDA
ESCL
N16
6
10
11
1
VCC
L3
L4
SO
Hall
17
INT
SI
3
SDA
SK
2
SCL
12
Res
16
Res
G1
18
OUT1
G2
19
OUT2
CS
7
LO
COP 842 CJ
G3
20
AL
CP+
9
CP+
L5
12
E(Ib)
L6
13
A(Iref)
CP-
8
CP-
L7
14
RGL
GND
CKO
CKI
15
4
5
GND
CKO
CKI

Fig. 10

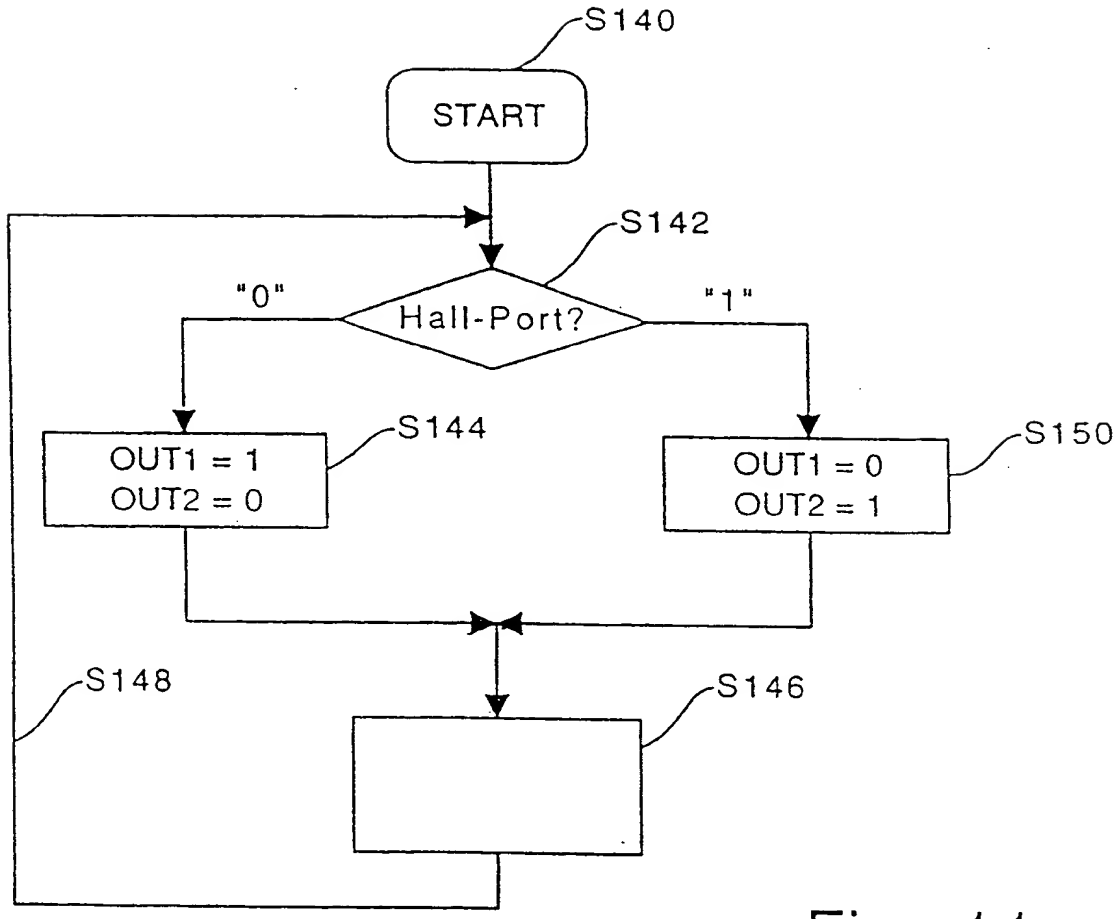
S140
START
S142
"0"
Hall-Port?
"1"
S144
OUT1 = 1
OUT2 = 0
S150
OUT1 = 0
OUT2 = 1
S148
S146

Fig. 11

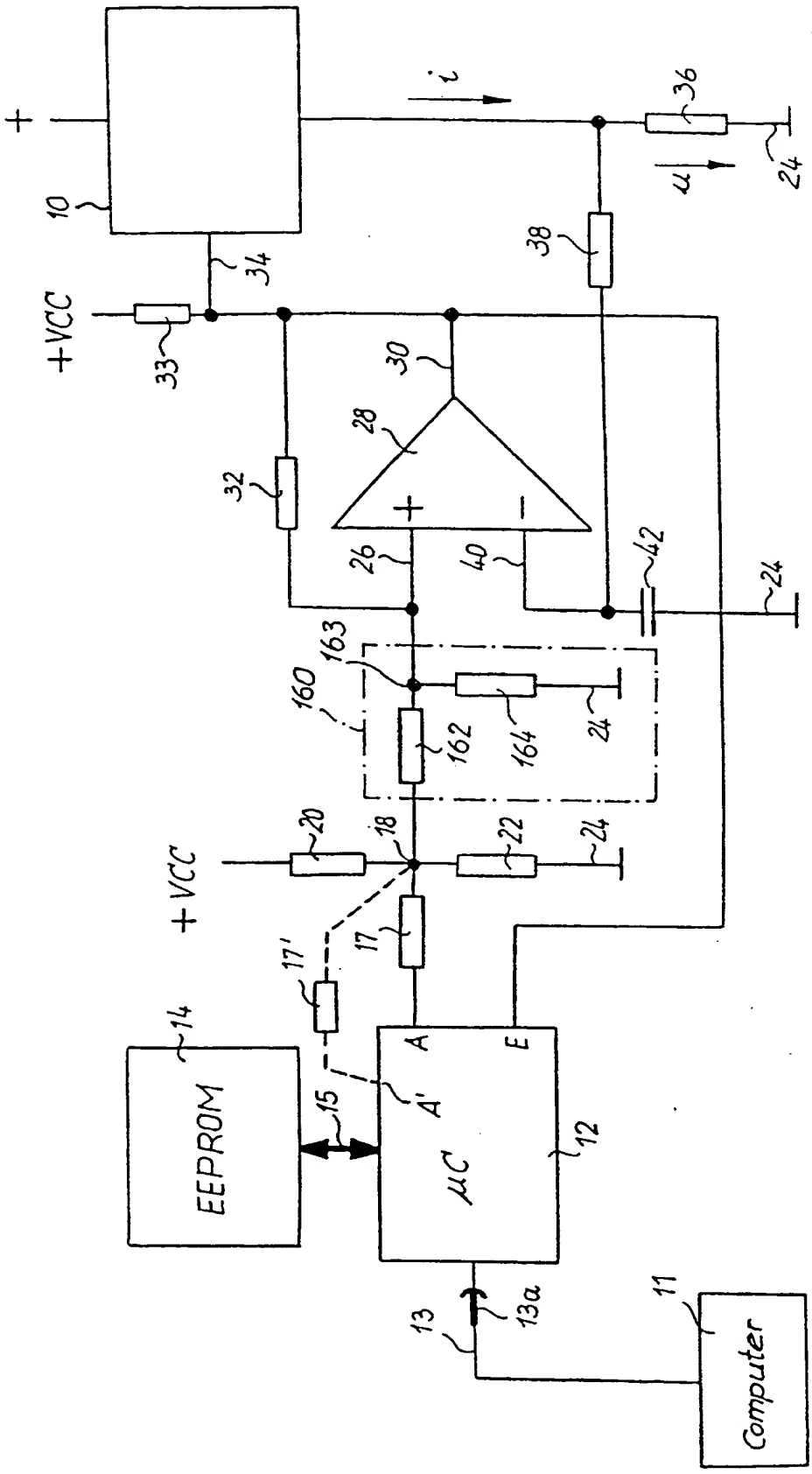
+
10
i
36
u
24
38
34
+VCC
33
30
28
32
26
40
42
24
163
160
162
164
24
20
18
22
24
+VCC
17
17'
14
EEPROM
15
A
A'
E
µC
12
13
13a
11
Computer

Fig. 12

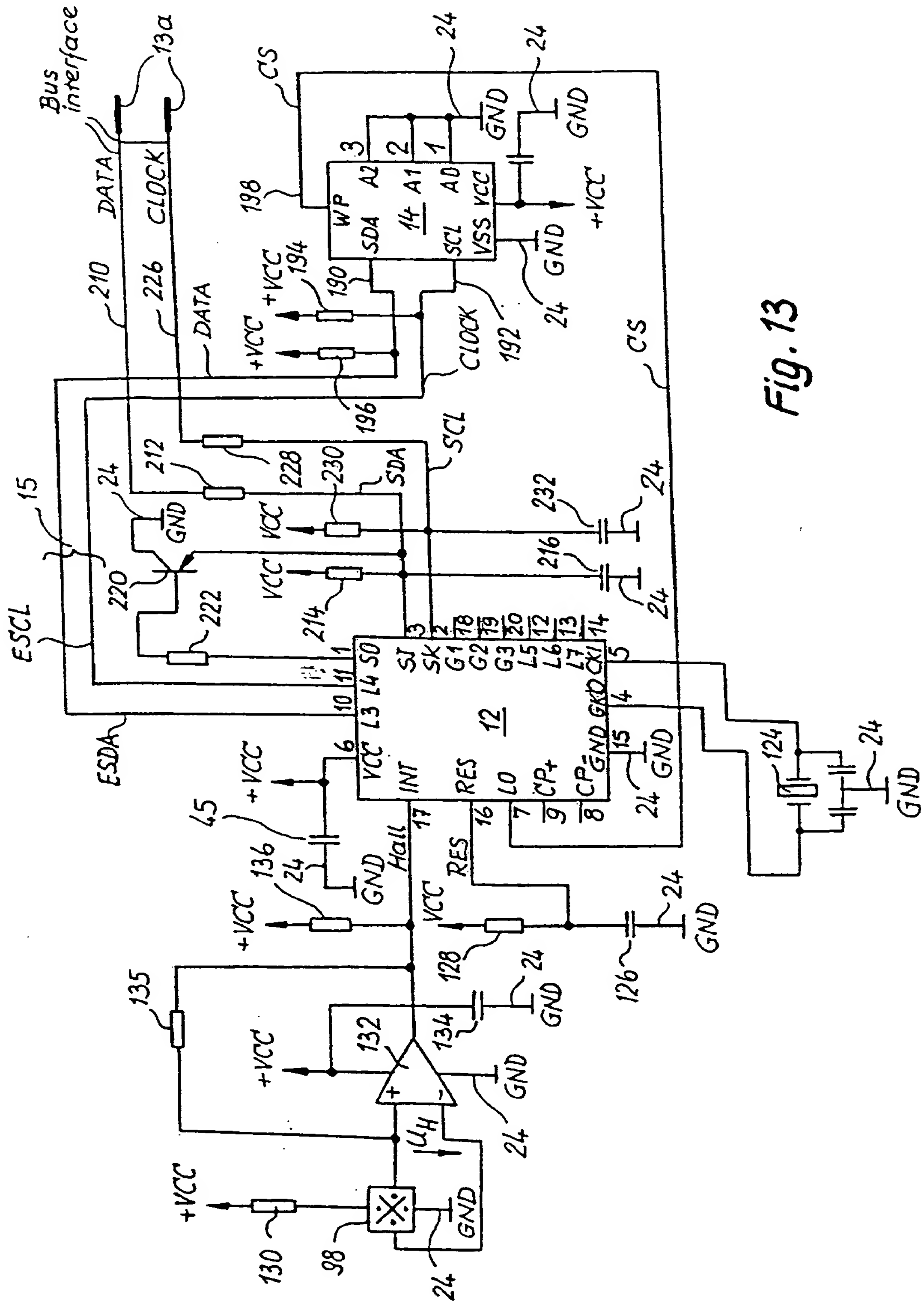
Bus interface
13a
DATA
CLOCK
CS
WP
SDA
A2
A1
A0
14
SCL
VSS
VCC
GND
+VCC
24
198
210
226
194
190
196
192
228
230
212
232
216
214
220
222
15
ESCL
ESDA
SDA
SCL
SI
SK
SO
L4
L3
G1
G2
G3
L5
L6
L7
CKI
CKO
12
INT
RES
LO
CP+
CP-
Hall
45
136
128
126
124
135
132
134
U_H
130
98

Fig. 13

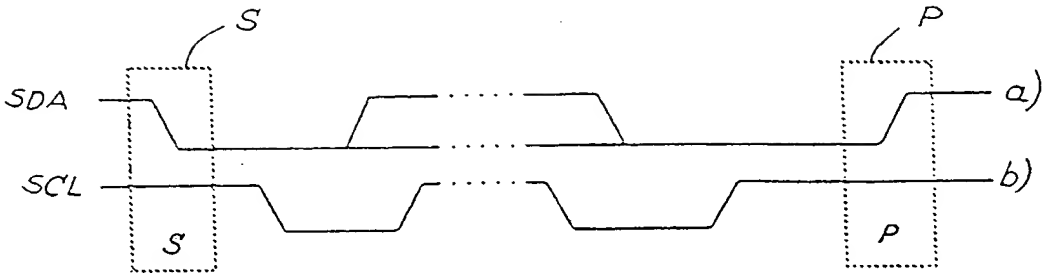

Fig. 14

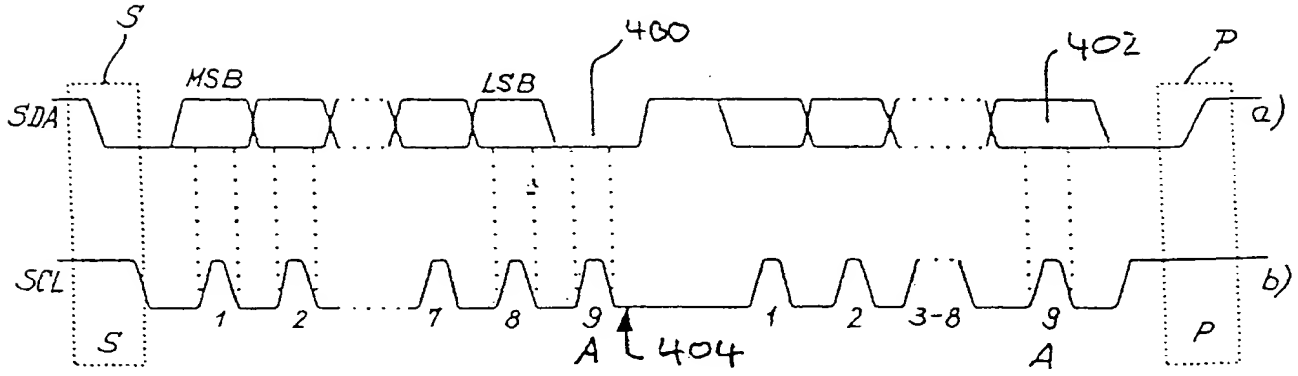

Fig. 15

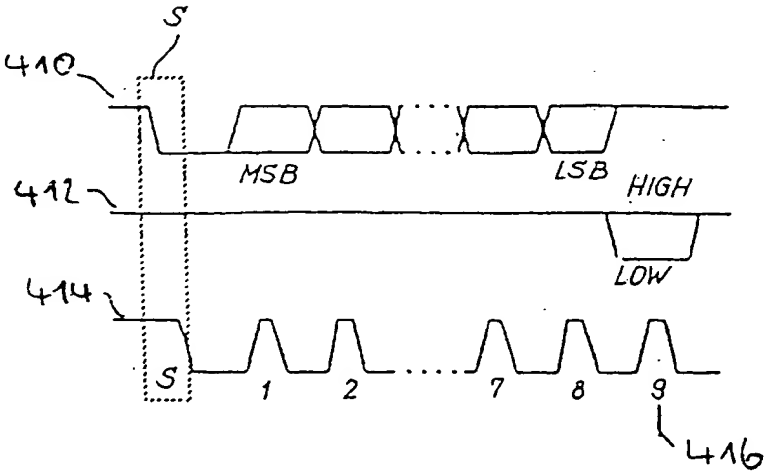

Fig. 16

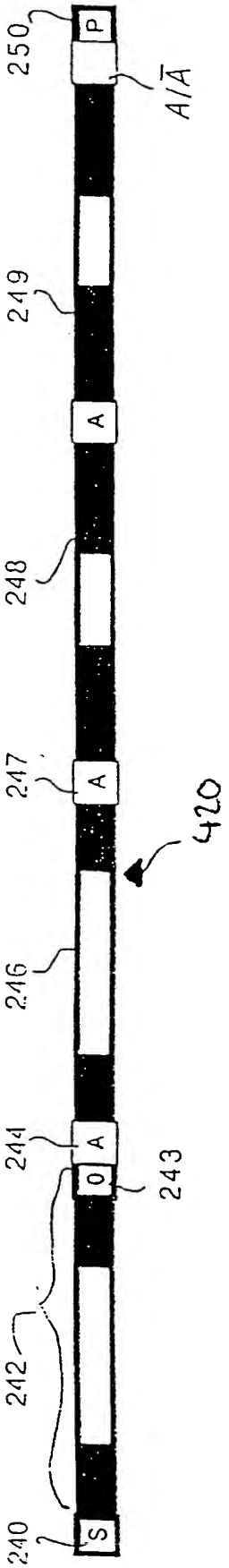

Fig. 17

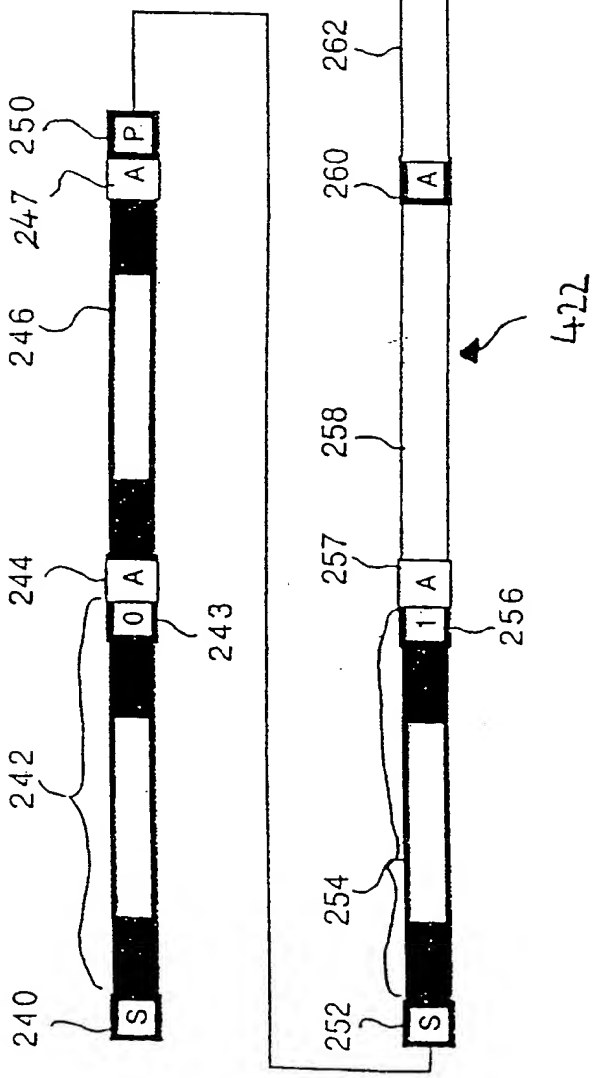

Fig. 18

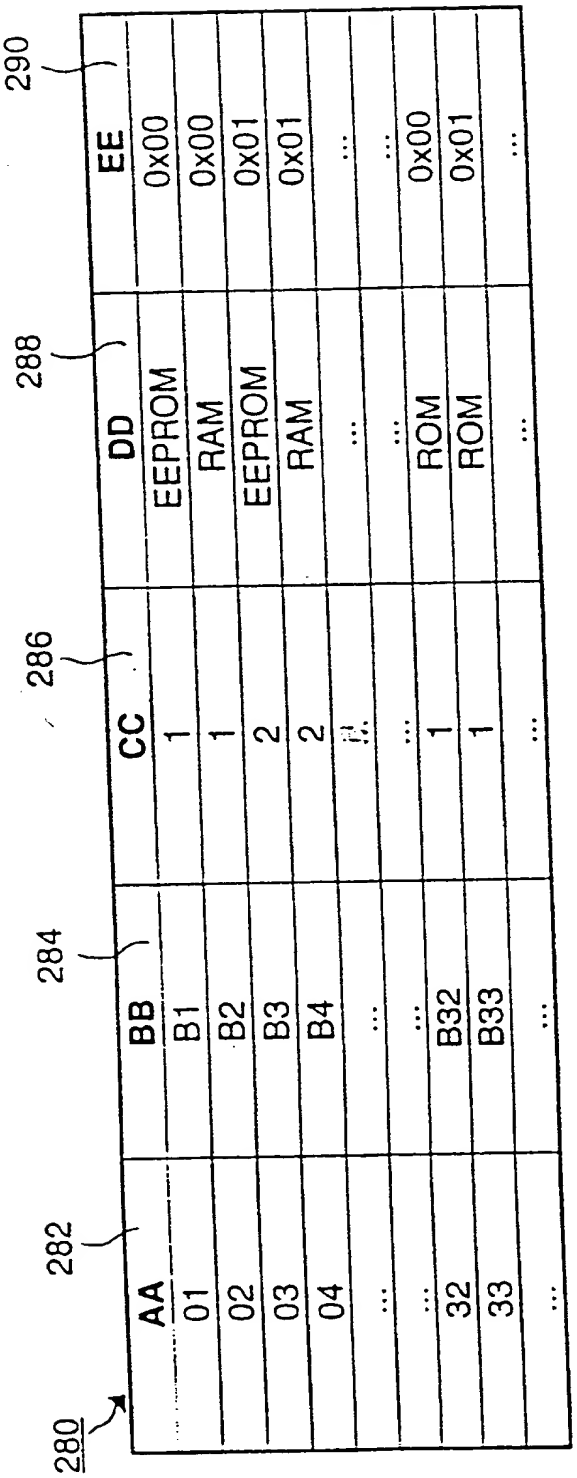
280
282
284
286
288
290
AA
BB
CC
DD
EE
01
02
03
04
32
33
B1
B2
B3
B4
B32
B33
1
2
EEPROM
RAM
ROM
0x00
0x01

Fig. 19

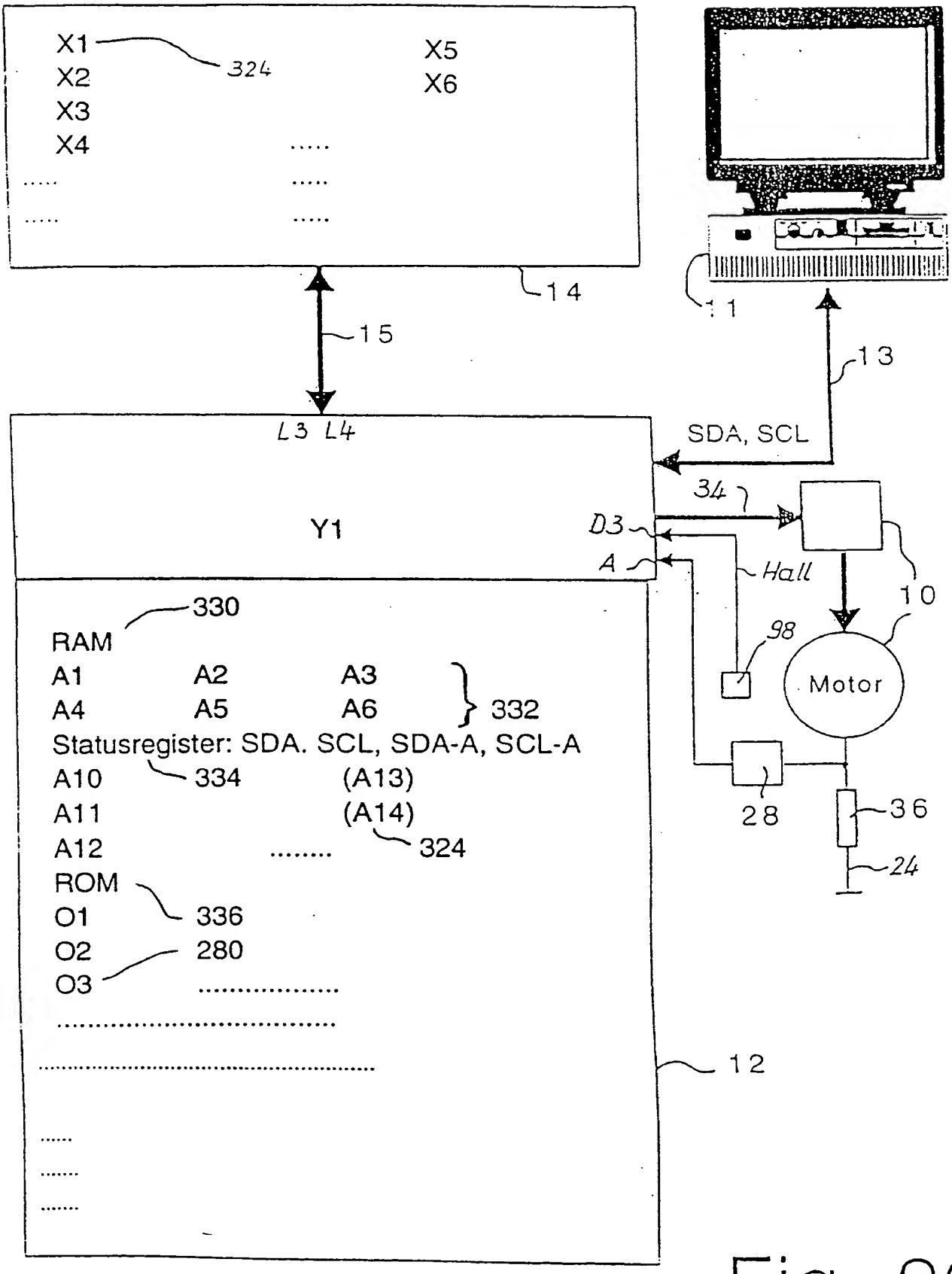
X1
X2
X3
X4
X5
X6
324
14
11
15
13
L3 L4
SDA, SCL
34
Y1
D3
A
Hall
10
98
Motor
28
36
24
330
RAM
A1 A2 A3
A4 A5 A6
332
Statusregister: SDA. SCL, SDA-A, SCL-A
A10 334 (A13)
A11 (A14)
A12 324
ROM
O1 336
O2 280
O3
12

Fig. 20

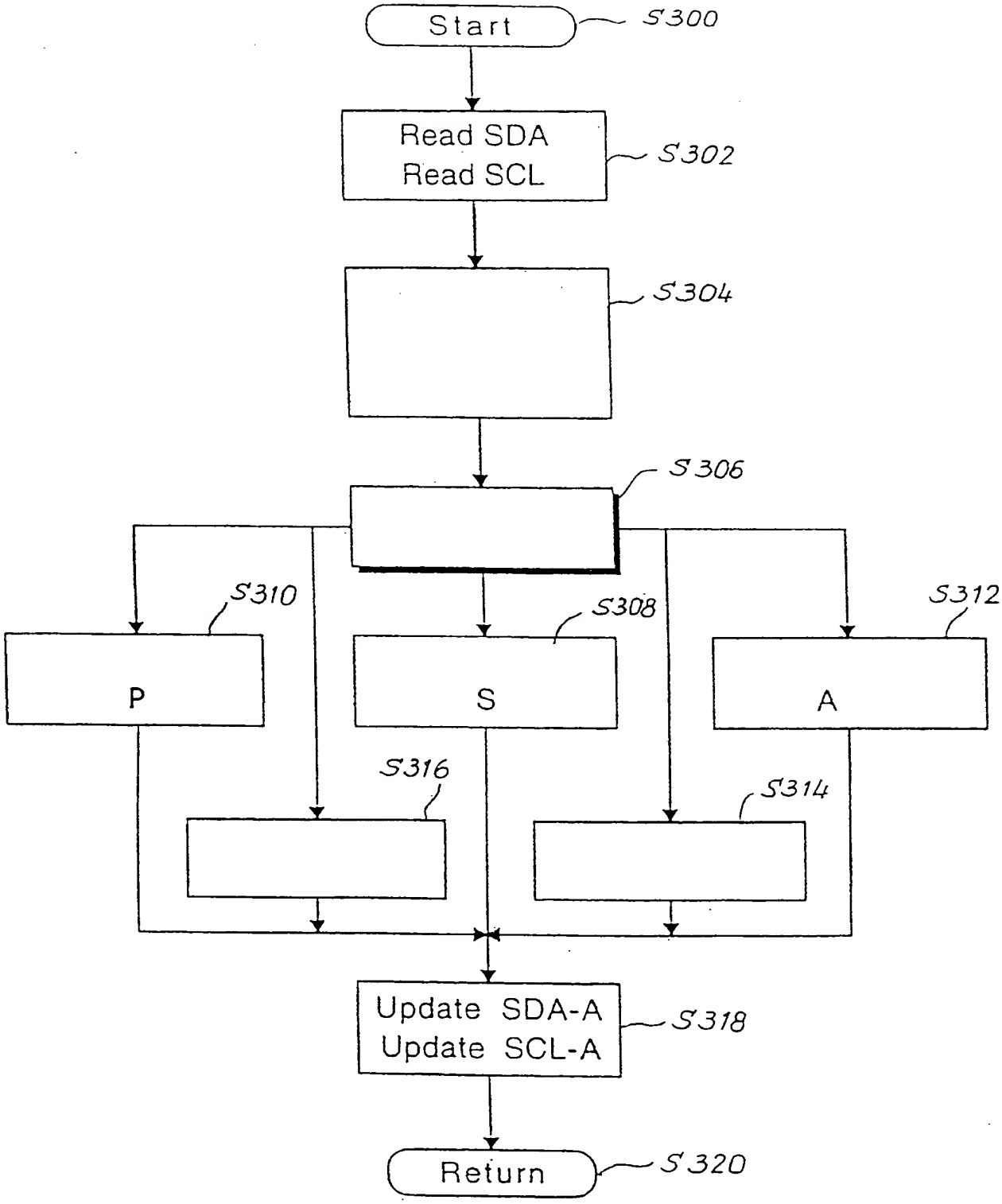
Start
S300
Read SDA
Read SCL
S302
S304
S306
S310
S308
S312
P
S
A
S316
S314
Update SDA-A
Update SCL-A
S318
Return
S320

Fig. 21

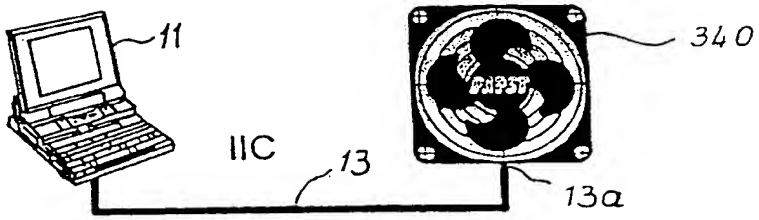
11
340
IIC
13
13a

Fig. 22

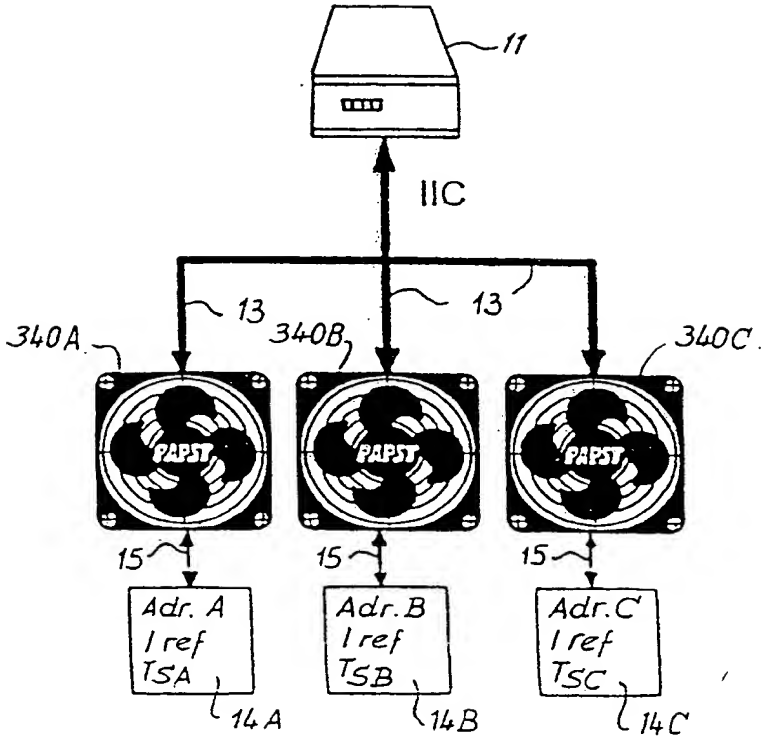
11
IIC
13
13
340A
340B
340C
15
15
15
Adr. A
I ref
TSA
Adr.B
I ref
TSB
Adr.C
I ref
TSC
14A
14B
14C

Fig. 23

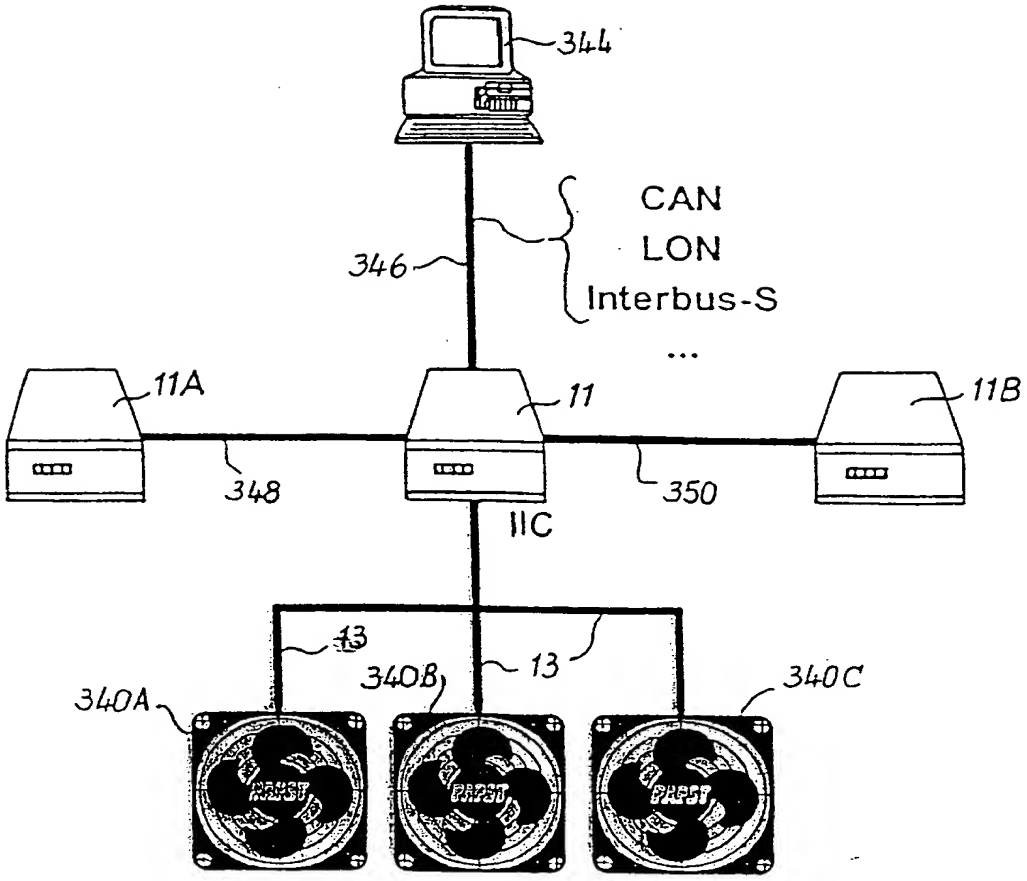
344
CAN
LON
Interbus-S
...
346
11A
11
11B
348
350
IIC
13
13
340B
340A
340C

Fig. 24